Full-Wave Modeling of Linear FETs for Millimeter Waves

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***Abstract*—Current monolithic-microwave integrated-circuit design, involving frequencies far in the millimeter and sub-millimeter ranges, is faced with the problem of the distributed nature of the devices. In this paper, we introduce a full-wave approach to the modeling of FETs under the small-signal hypothesis. The method is applied to MESFETs and pseudomorphic high electron-mobility transistor of different topologies and validated by comparison with available experimental data.**

***Index Terms*—Electromagnetic analysis, linear circuits, MESFETs, millimeter-wave FETs, MMICs, MODFETs.**

I. Introduction

MONOLITHIC-MICROWAVE integrated-circuit (MMIC) design is moving toward the millimeter- and sub-millimeter-wave bands due to the pressures of the consumer market, demanding larger bandwidths at lower costs, flexible telecommunication networks, as well as pressing for the development of the automotive radar.

At such high frequencies, building highly packed devices poses a number of difficult issues, e.g., the correct evaluation of the coupling between different devices, the modeling of "thick" lossy interconnecting lines, and the modeling of the interaction between traveling waves and charge carriers present in any active device. The latter problem arises when device dimensions are comparable to the signal wavelength at the operating frequency: accounting for the distributed nature of active devices is a key requirement for solving scaling problems and for understanding how a particular topology may affect device performance [1].

In the past, some efforts were devoted to the modeling of high-frequency active devices by using distributed equivalent circuits [2]–[4], while very few electromagnetic techniques were introduced and applied to simple structures [5], [6], the main limiting factor being posed by the cost of computational resources. Some authors also coupled the full-wave analysis of the passive periphery with a lumped equivalent circuit, derived by fitting measurements of an active finger, in order to be able to predict performances of multifinger devices [7].

However, this kind of approach may provide good results only if the standing waves arise at the periphery, while it is unable to predict, for instance, the optimum finger width since, along the fingers, the problem of standing waves may be even more severe, as demonstrated in [2].

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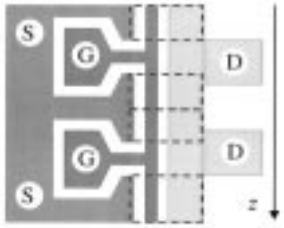


Fig. 1. Standard π-FET: dashed boxes identify active parts of the device.

Recently, the challenges of MMIC design have been the engine of the quest for so-called global modeling [8], including passive and active, often nonlinear, devices in a unitary framework.

Interest for such an ambitious aim has been encouraged by the availability of powerful desktop computers and the progress in numerical simulation.

In this context, we propose a frequency-domain procedure for the full-wave electromagnetic modeling of field-effect devices under the small-signal hypothesis. The proposed method allows the computation of the complete S-matrix of the device and a fast evaluation of the effects of scaling and of different topological choices: the algorithm is believed to be suitable for integration in computer-aided-design (CAD) packages for MMIC design.

This technique has been successfully applied to the modeling of several FET families and topologies; in this paper, results for commercial AlGaAs–InGaAs pseudomorphic high electron-mobility transistor (pHEMT) and standard GaAs MESFET are presented and validated by comparison with experimental data.

II. Theory

General Modeling Procedure

In this section, we provide an overview of the procedure followed in FET modeling, while discussing some important details in the following subsections.

As a first step, we separate the device in its passive parts (periphery) and active parts (fingers), both to be modeled by full-wave approaches. Fig. 1 shows, as an example, the scheme of a π-topology FET: the dashed boxes identify four identical active building blocks. There is some deal of freedom when selecting the width of the source and drain line of the active blocks; in principle, they ought to match the dimensions of the source and drain ohmic contacts, however, the gate line is usually the one dominating the propagative and lossy effects of the device,

through its cross-sectional dimensions and those of the underlying depletion layer. Hence, in order to reduce the computational load, it is possible—even if not necessary—to consider a reduced dimension for the source electrode. To some extent, this device may also be used for the drain electrode; however, in this case, the selection has to be much more careful, as the drain-to-gate capacitance is a key parameter for correctly predicting the transistor performances.

Modeling each active block under the small-signal (linear) assumption requires the following two additional steps:

Step 1) Modal computation (two-dimensional (2-D) problem).

Step 2) Computation of the network parameters.

As to step 1), we consider a structure uniform along the width direction (z), with the same cross section as the active block, including the active parts, namely the controlled current sources. For this structure, we determine just the three fundamental quasi-TEM modes; higher order modes may also exist for very high frequencies, but their influence on the overall analysis appears negligible.

Once the modal properties are known, Step 2) can be addressed. A single finger is treated as an actively coupled multiline supporting three quasi-TEM modes. For each mode, voltages between electrodes and currents over the electrodes are obtained and the scattering matrix S of a single finger, treated as a six-port (three input and three output ports of the multiline), is quickly evaluated.

The validity of the standard voltage definition for quasi-TEM modes in FET structures was carefully investigated in [5], resulting in negligible deviations up to more than 100 GHz when comparing voltage–current and Poynting-vector-based power definitions.

Finger discontinuities (if any) may be included in the passive parts of the structure and modeled in the next step. This may be important in some cases, such as for the inter-digital topology.

The next step, namely, modeling the passive periphery, involving bonding pads, wires, and possibly power splitters and combiners, may be performed by means of one of the available commercial software packages. In our study, we have used Microwave Office by AWR, which includes a standard spectral-domain electromagnetic simulator. This was possible owing to the relative large dimensions of the peripheral conductors, allowing, to an extent, to neglect the effect of conductor losses. If those losses are thought to play a relevant role, periphery can be modeled as in [9], or by a more effective and flexible approach exploiting the basic idea of [9], which will be the subject of future study.

Finally, combining the results of the previous steps at network level allows the simulation of the whole device. Note that, in order to investigate the effects of a different topology, or the consequences of scaling, such as involved in changing the finger lengths, it is not necessary to repeat step 1), which is the modal computation, which is, of course, the most time-consuming and critical process. In fact, changing the finger lengths will just require running step 2), while a different topology may require the simulation of the new periphery and the rearrangement of the whole network.

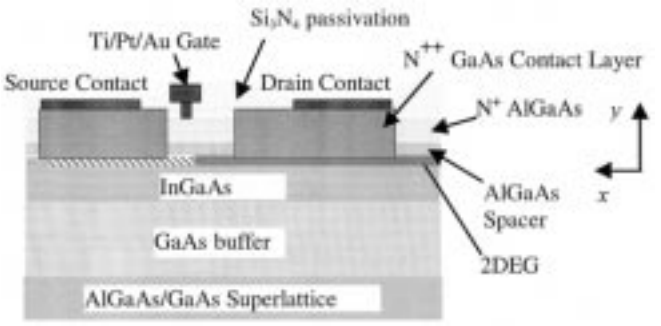


Fig. 2. Schematic view of the cross section of a single "mushroom" AlGaAs–InGaAs pHEMT active element. The structure is enclosed in a large box.

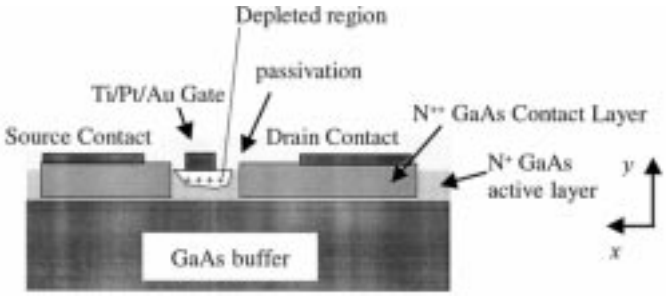


Fig. 3. Schematic view of the cross section of a standard GaAs MESFET active element. The structure is enclosed in a large box.

Modal Computation and FET Model Parameters

A critical step of the present method is the computation of the three fundamental quasi-TEM modes of a structure having the cross section of an active block, including the active parts, namely, the controlled channel sources. The general approach to the computation of the modes for structures of this kind is addressed in depth in [10], whereas, here, we provide just a short account of the method. Fig. 2 depicts the scheme of an pHEMT cross section, while Fig. 3 refers to a MESFET.

Basically, one has to calculate the dyadic Green's function (DGF) of the composite substrate of the device without conducting regions, say, $\mathbf{Z}$, linking the electric field to *volume* currents everywhere in the dielectric stack; some care is needed in order to evaluate the correct DGF in the source region [10]. Hence, the stack is defined by the set of layers homogeneous in the horizontal (x)-direction. Note that the DGF also accounts for losses in the dielectrics by the usual definition of complex permittivity.

Volume currents model the remaining conductor, semiconductor, and channel regions; the very nature of such currents is specified by imposing: 1) Ohm's law to be satisfied within the conductors and 2) the two-dimensional electron gas (2DEG) in high electron-mobility transistors (HEMTs) and the channel current in the epitaxial layer in MESFETs to be linearly controlled by the vertical (y-directed) field underneath the gate electrode.

Note that the second constraint yields a fully electromagnetic treatment of the *active* part.

Applying these two constraints yields the integral equation to be solved for the modes we are seeking. Before addressing this

issue, some further considerations are needed. In both MESFET and HEMT families, the gate electrodes form a Schottky junction with the underlying layer, but their behavior in the normal operating mode is rather different.

In the pHEMT of Fig. 2, the doped AlGaAs region may be assumed to be completely depleted, as is usually the case for normal HEMT operation in order to avoid parasitic paths between the source and drain [11]. The incoming electric field over the complete AlGaAs layer controls the density of the 2DEG. In the MESFET, on the other hand, the depletion region controls the width of the channel, modulating the total current flowing from source to drain. Due to the small-signal hypothesis, it is assumed the depletion cross-sectional dimensions are fixed, while the channel current density are modulated by the field across the depletion region. An important consideration has to be made as to the shape of the depletion region. Its form is important, as it strongly affects the static gate capacitance. On the other hand, in as far as dynamic effects are concerned, the cross-sectional dimensions are much smaller than the wavelength up to very high frequencies, far beyond the millimeter range. For this reason, the depletion region is modeled as an insulating layer, horizontally limited by the source and drain caps, and having a mean depth in order to accounting for the static gate capacitance.

A more accurate model of the shape of the depletion region is indeed possible by accepting a severe additional computational load, but in most practical cases, it does not result in any accuracy improvement. In fact, a direct correspondence between the differential gate capacitance, due to the charge accumulated in the depletion region, and the capacitance due to the field between the gate electrode and the channel exists only under the hypothesis of an abrupt passage from the ionized region to the channel layer and for vanishing drain-to-source voltage. In this case, a well-known property is that the simple parallel-plate expression for the gate capacitance [see (1) in the following] is formally the same obtained by differentiating the charge in the Schottky contact with respect to the gate-to-source voltage. Owing to these considerations, it is generally preferable to assume an effective depth for the depletion layer.

To this aim, it is important to estimate the static gate-to-channel capacitance per unit length: for micrometric gate electrodes, the common "parallel-plate" formula

$$C_{g_{\text{bott.}}} = \frac{\varepsilon_r \varepsilon_0 l_g}{t_{\text{depl.}}} \tag{1}$$

holds quite satisfactorily [2]. However, for submicrometric FETs, the contribution to the total capacitance of the sidewalls and, eventually, of the top surface of the gate electrode is generally not negligible (as shown, e.g., in [12] for a MOSFET). Equation (1) provides underestimated values, as highlighted in the schematic cross section shown in Fig. 4, where contributions to the total capacitance have been reported.

This effect is shown in Fig. 5, where the capacitance predicted by (1) is compared with the one obtained by an electromagnetic model. In the electromagnetic algorithm, the propagation constant and characteristic impedance of a metal–insulator–semiconductor (MIS) microstrip are determined at relatively low frequency and the parameters of an equivalent lossy line are optimized in order to fit the microstrip characteristic parameters. In

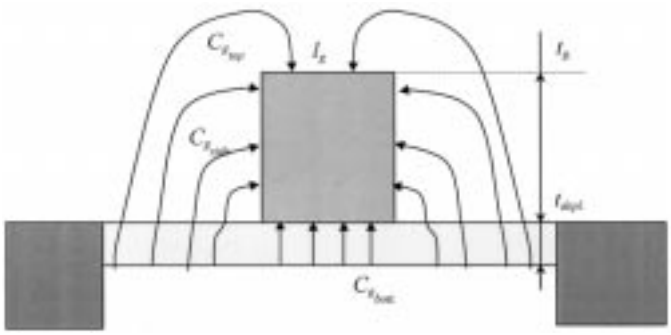


Fig. 4. Scheme of a gate electrode over a depleted layer, showing contributions to its total capacitance.

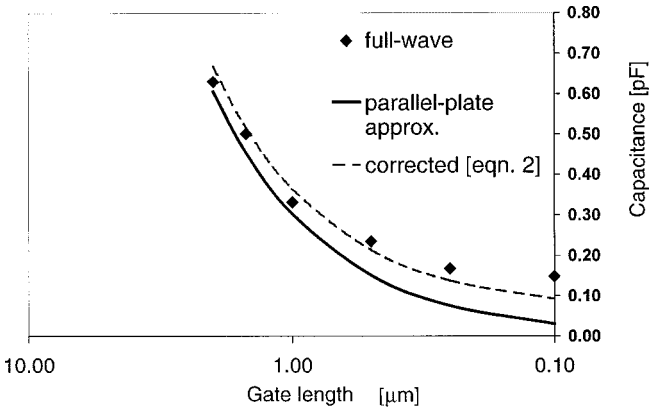


Fig. 5. Gate capacitance: comparison between parallel-plate approximation and electromagnetic results. Structure parameters: depletion layer 0.1-μm thick, electrode thickness 0.5 μm, $\varepsilon r = 12.2$, the electrode is embedded in an Si3N4 dielectric layer $(\varepsilon r = 7.5)$ and is 280-μm wide.

our study, the electromagnetic algorithm has been used in order to select the effective depth of the depletion layer and to model the gate differential capacitance; however, it is possible to correct (1) so as to widen its range of validity by adding a term roughly estimating the side capacitance.

By simply assuming a uniform circular electric field in the medium embedding the strip and approximating its lines of force as straight lines in the depletion region and by imposing continuity of the electric flux density across the boundary between the two regions, one obtains

$$C_{g_{\text{side}}} \approx \frac{2\varepsilon_0 \varepsilon_{r_{\text{cmb.}}}}{\pi} \ln\left(\frac{\pi \varepsilon_{r_{\text{depl.}}} t_g}{2\varepsilon_{r_{\text{cmb.}}} t_{\text{depl.}}} + 1\right). \tag{2}$$

The total gate capacitance per unit length is obtained by adding to (1) twice the value of (2). Thus, the improvement obtained is highlighted in Fig. 5. For T-shaped gates, some further (usually minor) corrections may be needed. Its amount is evaluated by calculating the capacitance of the upper part of the T-gate alone.

The needed differential static gate capacitance, as function of the bias point, may be obtained by using the nonlinear models, e.g., as in [13] for MESFETs and [14] for HEMTs. Note that, this way, the present model is able to completely predict performances of a device simply starting from structural parameters—virtually avoiding any fitting. However, to this aim, a detailed knowledge of the physical parameters is needed; these parameters are often not available, or at least they are not known to

the degree of precision necessary for a reliable simulation. On the other hand, measurements on a given sample may be available. In this case, the static gate capacitance is derived by fitting at the bias-point measured low-frequency S-parameters to the lumped equivalent circuit for the device. The advantage of the latter approach is that one does not have to distinguish between MESFET and HEMT devices, as the equivalent circuits share the same topology and the present method may still be used in order to analyze and predict scaling and topological effects. The same considerations apply to the modeling of SiGe devices.

The differential gate-to-drain feedback capacitance ($C_{\rm gd}$) also has to be considered. In the normal (saturation) operation of linear microwave FETs, it is nearly independent of the biasing point, reducing to the gate-to-drain interelectrode capacitance; hence, no further modeling is needed. Whenever the operating point does not completely satisfy the saturation hypothesis, an additional capacitance between gate and drain electrodes has to be added at the network level in the last step of our modeling approach, thus partially offsetting the truly distributed and full-wave nature of the model. The above drawback could be circumvented by adding an additional volume current source between the gate and drain and by specifying this to be a displacement current in a denser dielectric accounting for the increased capacitance according to

$$\mathbf{E}(\mathbf{r}) = \frac{\mathbf{J}(\mathbf{r})}{j\omega\varepsilon_0\big(\tilde{\varepsilon}(\mathbf{r}) - \tilde{\varepsilon}'(\mathbf{r})\big)}. \tag{3}$$

Equation (3) is imposed in the gate-to-drain interelectrode region, $\tilde{\varepsilon}$ is the complex permittivity of the additional dielectric, while $\tilde{\varepsilon}'$ is the one of the medium embedding the strips. This constraint has been used in [15] in order to model horizontally limited dielectric regions in a classical spectral-domain framework.

With a view to model velocity saturation of the carriers, the active channel is divided into two regions: a high-conductivity area between the gate and source and a lower conductivity region (saturation region) between the gate and drain, as shown in Fig. 2 for the HEMT. The highly conducting region is responsible for the intrinsic gate-to-source resistance R_i. Its resistivity is linked to the latter parameter as follows:

$$\rho_h \approx \frac{R_i h w}{l_g + l_{\rm gs}} \tag{4}$$

where $l_{\rm gs}$ is the distance between the gate electrode and source cap, W is the device width, and h is the depth of the undepleted part of the channel for MESFETs and the 2DEG thickness for HEMTs.

The saturated low-conductivity part of the channel is responsible for the differential output resistance of the FET as follows:

$$\rho_l \approx \frac{R_{\rm out} h w}{l_{\rm gd}}. \tag{5}$$

$l_{\rm gd}$ being the distance between the gate electrode and drain cap. Values for ρ_l and ρ_h may also be directly obtained from the saturated and linear values of the carrier mobility, when available from Hall measurements, i.e.,

$$\rho_{l,h} = \frac{1}{qn\mu_{l,h}} \tag{6}$$

where q is the unit charge, n is the carrier density, and μ is the carrier mobility. Note that, when using (6) in MESFETs, a slight correction may be needed in order to account for the layered model of the depletion region.

Once the physical and geometrical properties of the device cross section are fully specified, we proceed by imposing the constraints onto the volume currents, namely, Ohm's law

$$\mathbf{J}(\mathbf{r}) = \sigma(\mathbf{r})\mathbf{E}(\mathbf{r}) \tag{7}$$

to hold in the horizontally limited conductors and semiconductors and the channel (or the 2DEG) controlled current to be

$$\mathbf{J}(\mathbf{r}) = \mathbf{G}\big(\mathbf{r}, \mathbf{r}'\big) \cdot \mathbf{E}\big(\mathbf{r}'\big) + \sigma(\mathbf{r})\mathbf{E}(\mathbf{r}). \tag{8}$$

By combining constraints (7), (8), and possibly (3) in the field-to-current relationship, one obtains the integral equation

$$\int d\mathbf{r}''\Bigg\{\mathbf{G}\big(\mathbf{r}, \mathbf{r}'\big) \cdot \mathbf{Z}(\mathbf{r}', \mathbf{r}'', \gamma) + \Big[\sigma(\mathbf{r}) + j\omega\varepsilon_0\big(\varepsilon(\mathbf{r}) - \varepsilon'(\mathbf{r})\big)\Big] \cdot \mathbf{Z}\big(\mathbf{r}, \mathbf{r}'', \gamma\big) + \mathbf{I}\big(\mathbf{r}, \mathbf{r}''\big)\Bigg\} \cdot \mathbf{J}\big(\mathbf{r}''\big) = \mathbf{0} \tag{9}$$

where $\mathbf{I}$ is the identity operator, while σ is the conductivity of the region being considered. The operator $\mathbf{G}$ is the one linking the controlled source to the controlling field. Its domain is the Schottky contact, being nonvanishing just in the 2DEG or, more generally, in the channel. An approximate expression for $\mathbf{G}$, as derived in [10], is

$$\mathbf{G}(\mathbf{r}, \mathbf{r}') = \frac{g_m}{wd} e^{-j\omega\tau} e^{-\gamma(z-z')} \delta(x') \mathbf{xy}$$

where w is the device width, d is the channel depth, τ is the time delay, g_m is the static transconductance, and γ is the unknown modal propagation constant. As assumed for the gate capacitance, the static transconductance may either be obtained from a physical model or from low-frequency measurements of a given sample.

General expressions for $\mathbf{Z}$ may be found in [10].

Integral equation (9) is solved by the Galerkin method, obtaining for each mode the propagation constant γ and the current distribution. Piecewise constant functions are used to expand all the current components (J_x, J_y and J_z) in both the x- and y-directions, with the only exception of the currents J_x in the source, gate, and drain. The latter are expanded in the x-direction by rooftop functions in order to reduce the risk of spurious solutions.

Network Parameters

By defining standard voltages to ground (the box) and currents—given by direct integration of the obtained current densities—for each mode, terminal voltages and currents are expressed as their superposition

$$V_i(z) = \sum_{n=1}^{3} v_i^{(n)} \Big[A_n e^{-\gamma_n z} + B_n e^{\gamma_n z}\Big]$$

$$I_i(z) = \sum_{n=1}^{3} i_i^{(n)} \Big[A_n e^{-\gamma_n z} - B_n e^{\gamma_n z}\Big], \qquad i = s,\, g,\, d. \tag{10}$$

In the above , A_n and B_n are unknown excitation amplitudes, whose elimination provide the Z-matrix and, after simple manipulation, the S-matrix of the structure. Hence, the single active element is modeled by means of a six-port network.

III. Results

AlGaAs–InGaAs pHEMT

The modeling procedure has been applied to several FET structures. In this section, we report as an interesting example the simulation of a Filtronic pHEMT Lp7512 over the 1–50-GHz band, and the comparison with available measured data.

Structural data are partly obtained from [11] and partly from the manufacturer data sheet. This device features a recessed "mushroom"-type 0.25-μm gate, being a 200-μm-wide π-topology pHEMT; the conductors are embedded in an Si_3N_4 passivation layer. Its topology is depicted in Fig. 1.

According to step 1) in Section I, four identical active fingers, 50-μm wide, are identified. Fig. 2 shows how a single finger of this structure is represented. The $\mathbf{G}$ operator was built from the static transconductance of the device.

The modal computation for 50 frequency points and three quasi-TEM modes required about 4 h on a standard 233-MHz Pentium II processor.

Dispersion and attenuation for the three fundamental modes of the structure are reported in Fig. 6 for $V_{gs} = -0.34$ V and $I_d = 10$ mA. The attenuation of the two of them decreases over a limited frequency range due to the interaction with the 2DEG.

Once the current distributions and complex propagation constants are determined, the S-parameters of a single finger are obtained in a few minutes.

The whole analysis is completed by arranging the network representations and including periphery, parasitic, and bonding wire effects.

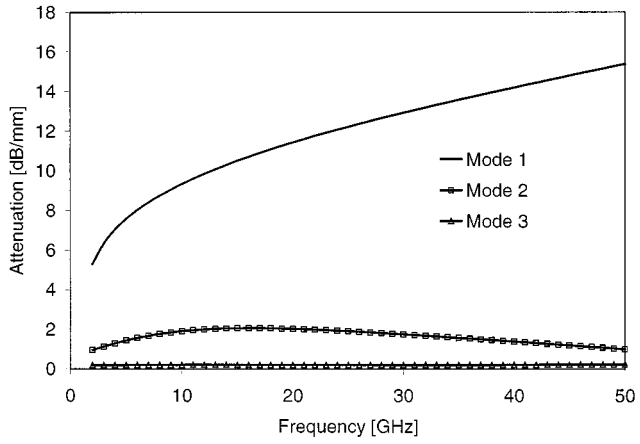
Fig. 7 shows this arrangement where, just for the sake of simplicity, networks simulating the periphery and bonding wires have been collected together in equivalent lumped elements; in this particular case, this choice had a rather negligible effect on the results.

Fig. 8 shows the comparison between theoretical and experimental data for the maximum stable gain (MSG), the maximum available gain not being definable due to the conditional stability of the device over the whole frequency range.

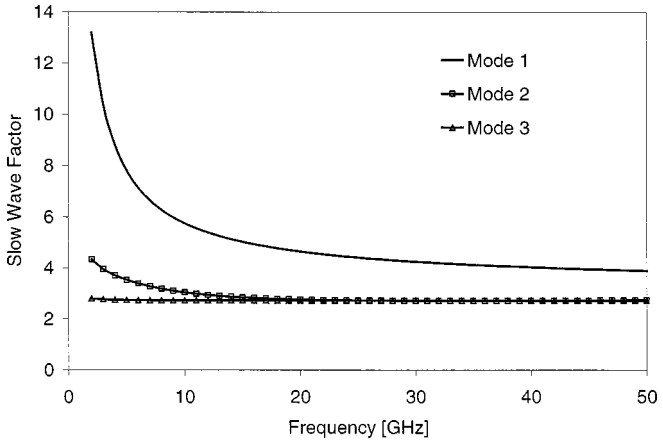
In Fig. 9, we have reported on the magnitude of the S-parameters for both theoretical and experimental data: the agreement is good in all cases, and the difference between simulated and measured data is within the limits of repeatability of the device parameters [11].

Fig. 10, reporting a polar plot of the S_{21}, shows a good agreement even for the phase, and the same holds for the remaining S-parameters.

The question may be raised about the relative accuracy of the proposed approach with respect to traditional lumped-element approach. Fig. 11 shows the Rollett stability factor, as compared with experimental data and data obtained by an equivalent lumped-element circuit, as indicated in the manufacturer data sheet.



(a)



(b)

Fig. 6. Slow-wave factor and attenuation for the three fundamental modes of the pHEMT in Fig. 2.

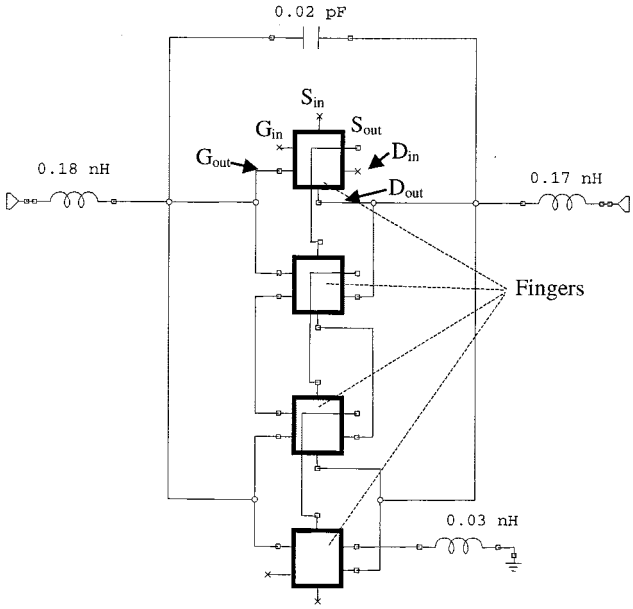


Fig. 7. Network arrangement for the characterization of the whole device of Fig. 1.

It appears that while the equivalent circuit does provide an excellent agreement in the lower frequency range—where it

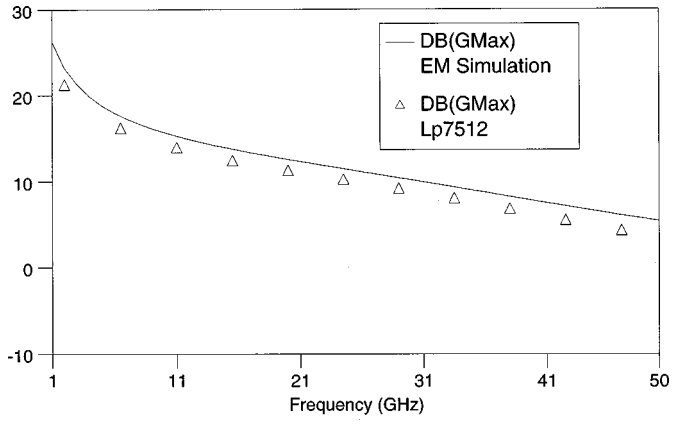


Fig. 8. MSG: comparison between theoretical and experimental data.

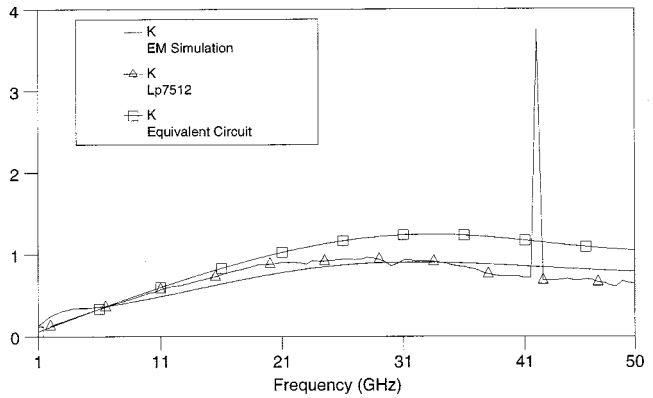


Fig. 11. Plot of the Rollett stability factor. Comparison between present method, lumped-element equivalent circuit, and experimental data.

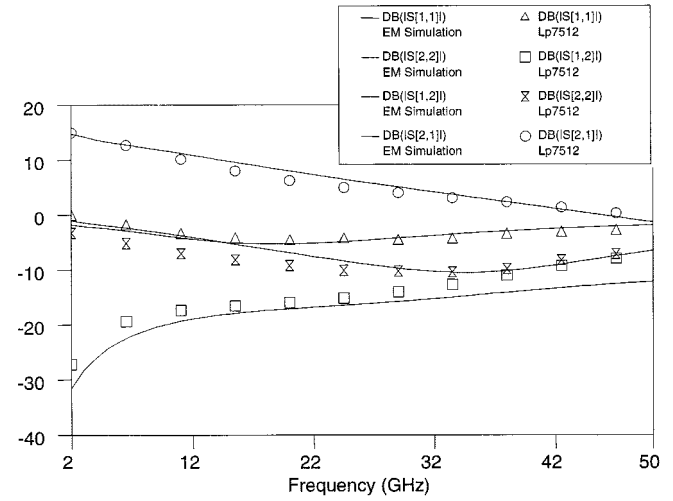


Fig. 9. Magnitude of the S-parameters for the pHEMT Lp7512. Comparison between theoretical and experimental data.

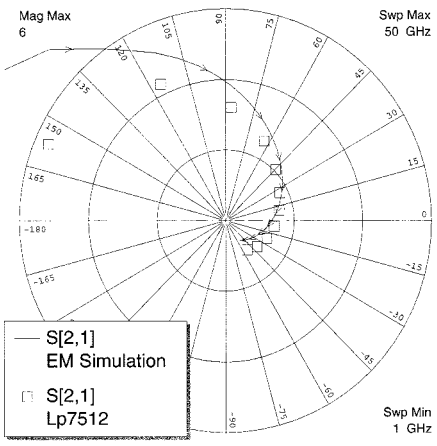


Fig. 12. Scaling effect on S_{21}. Comparison between theoretical data for a larger version of the LP7512 (400 μm) and data by Lp7512.

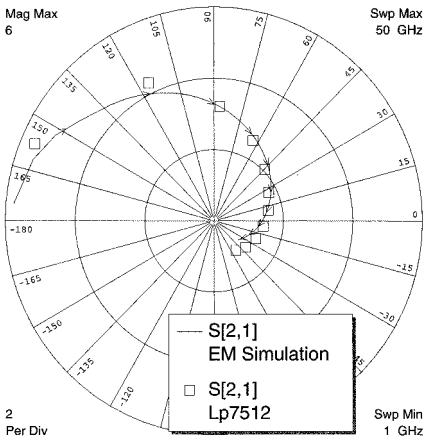


Fig. 10. Polar plot of S_{21} parameter. Comparison between theoretical and experimental data.

was optimized in order to fit within the measured data—it predicts an unconditional stability over 21 GHz. On the other hand, both the electromagnetic simulation and measured data highlight just a conditional stability all over the considered band. This results from the fact that the electromagnetic approach is self-consistent and it becomes increasingly accurate with higher frequency.

It should be stressed anyway that while the lumped equivalent circuit was obtained by *fitting* from the measured data, the electromagnetic simulation just relies on structural and physical parameters and *predicts* the device behavior all over the frequency range. Another key point is that there is generally an optimum finger width providing the best performances, as shown in [5], mostly influenced by changes in the transconductance, the gate and the gate-to-drain capacitances, and possibly, by standing waves arising over the finger itself. The present approach, due to its distributed nature, is able to deal with this optimum problem, what is beyond the possibility of any lumped-circuit approach, and of hybrid approaches like [7].

As an interesting test case, Fig. 12 shows what would happen if the same device were enlarged by doubling the width of its two side active areas, i.e., by stretching them up to a total width of 400 μm. According to the electromagnetic simulation, the S_{21} parameter would increase strongly at the lower frequency range and decrease above 27 GHz. The device would become unconditionally stable above 40 GHz and the gain would sharply decrease above this frequency. These effects are what common

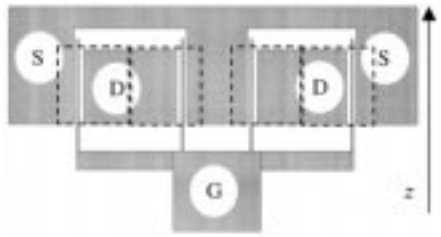


Fig. 13. Multifinger FET. Dashed boxes identify active parts of the device.

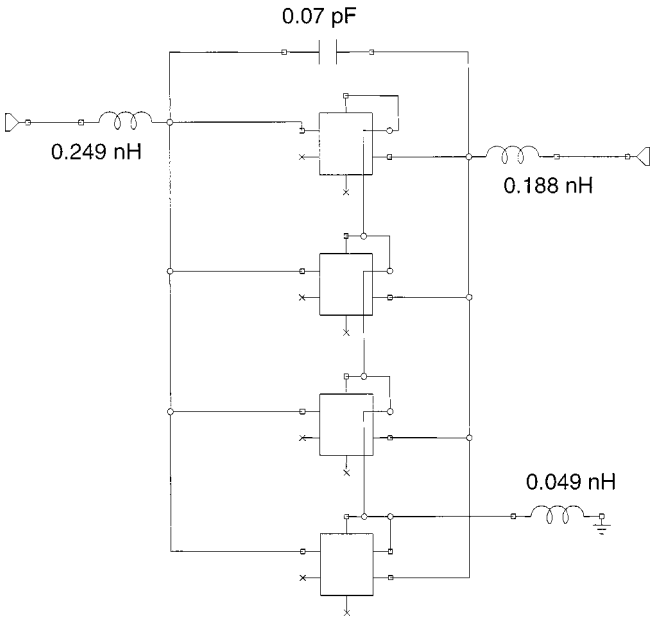


Fig. 14. Network arrangement for the characterization of the whole device of Fig. 13.

sense suggests as, on the one hand, the total transconductance is increased, thus increasing S_{21} at low frequency, while on the other hand, the gate capacitance is also increased, limiting the high-frequency performance.

Propagation effects along the FET width may be evaluated from Fig. 6. The slower mode has a slow-wave factor $\lambda_0/\lambda \approx 5$ at 50 GHz, so that its wavelength is about 1.2 mm, which is three times the device width. Consequently, we may expect the propagation phenomena to play some role in the behavior of the larger FET in the higher end of the frequency band considered, at least for the assumed bias. Reducing the gate voltage would result in increasing the gate capacitance, leading to a slower mode.

GaAs MESFET

The modeling procedure was applied to a multifinger GaAs MESFET, whose layout scheme is reported in Fig. 13: an NEC NE76100, biased at $V_{\rm ds} = 3$ V, $I_d = 10$ mA.

NE76100 is a 1-μm gate FET having a total width of 400 μm. According to our modeling procedure, in Fig. 13, four active fingers, 100-μm wide, are identified. Fig. 3 shows a scheme of the elementary cross section. Once obtained, i.e., the modal behavior and six-port network representing a single active finger, four building blocks are arranged, as depicted in Fig. 14, including bonding wires.

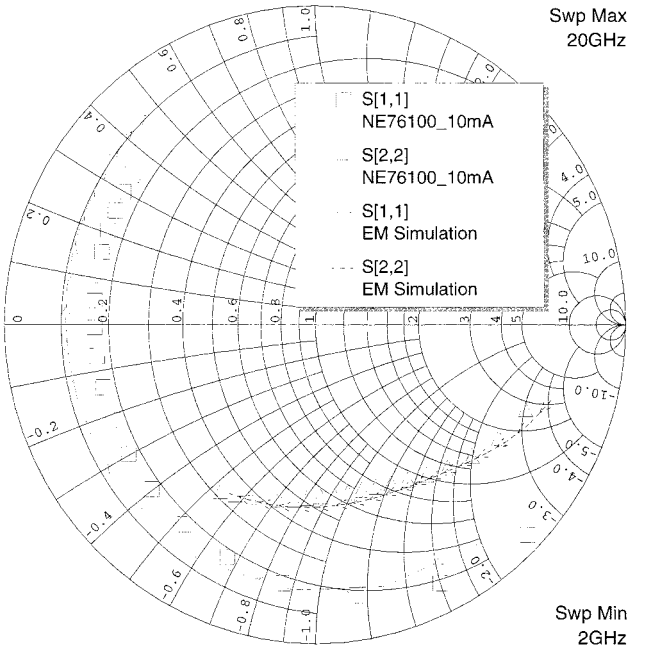


Fig. 15. Smith chart for S_{11} and S_{22} for MESFET NE76100. Comparison between theoretical and experimental data.

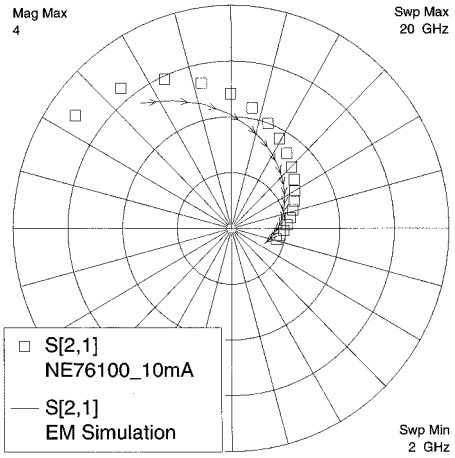


Fig. 16. Polar plot for S_{21} MESFET NE76100. Comparison between theoretical and experimental data.

The power splitter linking the gate pad to the gate electrodes was simulated, but due to the relatively low frequency at which the device does operate, its influence on the overall performance was found to be rather negligible; thus, it was omitted for the sake of simplicity.

Fig. 15 shows a Smith-chart plot for S_{11} and S_{22}, while Fig. 16 shows a polar plot of S_{21}. The comparison with the experimental data is good, even if slightly worse than for the previous example, mainly due to some structural parameters unknown to the authors. Even in this case, the device was found to be only conditionally stable over the frequency range considered. Fig. 17 reports the MSG obtained for this device.

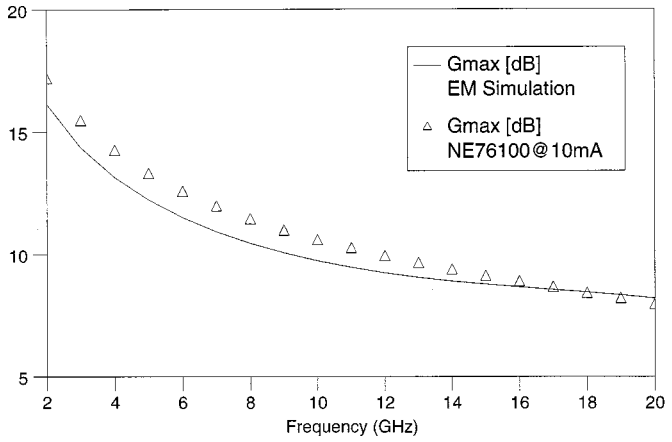


Fig. 17. MSG for MESFET NE76100. Comparison between theoretical and experimental data.

IV. Conclusions

In this paper, a new and promising approach to the modeling of high-frequency state-of-the-art FETs has been introduced. The method was applied to a number of commercial devices, giving encouraging results. Among them, the examples of an AlGaAs/GaAs mushroom-gate pHEMT and of a GaAs MESFET have been reported. The approach is self-consistent, and is able to predict device performances by starting form structural, geometrical, and physical parameters—namely, virtually no fitting is needed at all.

The proposed approach is generally not excessively time consuming and could be effectively used in the design of low-noise FET devices. Scaling and topological effects are easily evaluated.

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